**TITLE**: **AES Encryption and Decryption**

**ABSTRACT:**

One of most popular algorithms of cryptography is AES (Advanced Encryption Standard), which has data block of 128 bits and key size is variable of 128 bits, 192 bits and 256 bits. In this Project, I want to implement AES algorithm with a key size of 128 bits using Verilog in EDA playground tool. The primary idea is to construct individual blocks in algorithm and integrate them to bring out the functionality. The module takes key as well as plain data as inputs and gives out the cypher text which is encrypted. AES has more privacy and security compared to DES (Data Encryption Standard), because of its longer key size.

**EXPECTED OUTCOMES:**

* **Implementation of encryption and decryption logic:** 
  + Encrypted logic will generate cypher text and decrypted logic would give out the same data which is given as an input in encrypted logic. The cypher text would be the same as plain text such that 128 bits.
* **Understanding of Cryptography Concepts:**
  + Learn about the AES algorithm, its key expansion, and its different modes of operation.
* **Programming Skills:**
  + Improve programming skills by implementing AES encryption and decryption algorithms in Verilog.
* **Simulation results:**
  + Include the results of simulation such as delay and other parameters.
* **Real-world Application:**
  + In real time applications involving transfer of data, it improves security. It is almost impossible to decode AES encrypted code without the right key.
* **Protection of files from unauthorized access.**